20. (Amended) The method of claim 15, further comprising each memory controller determining when to generate a memory request based on the monitoring.

21. (Amended) The method of claim 15, further comprising each memory controller determining if a lock has been asserted due to presence of a read-modify-write transaction.

22. (Amended) The method of claim 15, further comprising each memory controller performing a cache coherency action based on the monitoring.

Add the following claims:

24. (New) The system of claim 1, wherein the plurality of memory controllers are connected to the memory bus.

25. (New) The system of claim 1, wherein one of the at least two memory controllers is adapted to generate its memory request on the memory bus before data is returned for the memory request of the other one of the at least two memory controllers.

26. (New) The system of claim 10, wherein at least two of the memory controllers are adapted to generate concurrently pending memory requests on the memory bus.

27. (New) The system of claim 26, wherein one of the at least two memory controllers is adapted to generate its memory request on the memory bus before data is returned for the memory request of the other one of the at least two memory controllers.

28. (New) The method of claim 15, wherein generating the requests on the memory bus comprises at least two of the memory controllers generating concurrently pending requests on the memory bus.

29. (New) The method of claim 28, wherein generating concurrently pending requests comprises one of the at least two memory controllers generating its request before data is returned for the request of the other of the at least two memory controllers.

30. (New) The article of claim 23, wherein the memory controllers are connected to the memory bus.